APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: COMPACTING CIRCUIT RESPONSES

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COMPACTING CIRCUIT RESPONSES

Background

This invention relates generally to integrated circuits.

Integrated circuits include input pins for receiving signals from the outside world and output pins for providing

5   signals to the outside world. Since integrated circuit packages are advantageously compact, increasing the number of pins means increasing the integrated circuit packaging size and cost.

For example, when testing integrated circuits, a number

10 of modules or components may be scanned or analyzed for errors or defects. The more scan chains of modules to be analyzed, generally the more pins that are needed to receive signals from those scan chains. Conversely, the longer the scan chains, the slower the testing process. Either way, the costs

15 may be aggravated.

Some of the major contributors to integrated circuit test cost include: available tester memory, available number of tester channels, test time, and number of pins available for scan-in and scan-out purposes. All these contributors to test

20 cost have direct relationships with the scan chain lengths and the number of scan chains.

Therefore, there is a need for better ways to compact circuit outputs to reduce the number of circuit pins or connectors without increasing the size of the circuit elements.

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Brief Description of the Drawings

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Figure 1 is a schematic depiction of one embodiment of the present invention;

Figure 2 is a partial depiction of one embodiment in accordance with Figure 1;

10   Figure 3 is a partial depiction of a matrix in accordance with the embodiment shown in Figure 2; and

Figure 4 is a flow chart for one embodiment of the present invention.

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Detailed Description

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15   Referring to Figure 1, a response compactor 10 may include scan in chains 12, identified as chains 1 through n. The circuit elements comprising the scan in chains can be any of a variety of circuit elements, components, or modules. The circuit outputs or scan outs 1 through n,

20   from the scan in chains 12, may be compacted by a combinational compactor 14 to produce outputs 1 through m, where m is significantly less than n. In this way, the number of circuit outputs may be reduced to a manageable level. For example, the compaction of the number of

25   circuit outputs may reduce the number of output pins,

reducing the cost of the resulting hardware in one
embodiment.

In some embodiments of the present invention, a large
number of test errors in scan chains may be handled. Also,
5 a large number of unknown logic values can be accommodated.
Thus, a relatively cost effective design that can handle a
large number of scan errors and unknown logic values may be
achieved in some embodiments.

In the ensuing discussion, examples are provided in
10 connection with circuits for testing integrated circuits. In
such cases, a scan chain may be analyzed by providing a
stimulus to the scan chain and receiving its output. In many
complex integrated circuits, a large number of scan chains may
each be provided with a stimulus. The responses of those scan
15 chains may be collected. In accordance with some embodiments
of the present invention, the number of outputs that are
provided to pins or other connectors may be reduced using a
response compactor 10. However, the present invention is not
limited to testing embodiments and is applicable to a wide
20 variety of integrated circuits.

Some of the scan chains can produce logic values unknown
during simulation (often called X-values) at the same scan-out
cycle when some other scan chain produces an error. In that
case, there is a chance that this error can get masked and the
25 defect is not detected.

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Referring to Figure 2, in accordance with one embodiment of the present invention, the scan ins 1 through n are indicated at 12 and they may be coupled to a response compactor made up of exclusive OR (XOR) gates 14 in one

5   embodiment. While an embodiment using a combinational compactor is shown, embodiments using sequential compactors may also be used by the duality between space versus time compression. Also, flip-flops or other devices may be used instead of XOR gates 14.

10   The matrix representing the embodiment shown in Figure 2 is illustrated in Figure 3. Thus, the output 1 is created from an exclusive OR gate 14 from scan ins 1 and 2, because a one is indicated in each row under output 1 for scan ins 1 and 2. Similarly, scan ins 3 and 4 are provided

15   at output 2 through another exclusive OR gate 14 because of the ones indicated in the second column of the matrix shown in Figure 3.

In order to develop the compactor 10, the designer determines the maximum number of scan chains that can

20   produce unknown logic values at the same time. This number may be assigned the value K. Also, the designer determines the total number of scan chains and assigns the value N to that number. If there are K unknown logic values, N - K error-free outputs each have at least one path to a

25   compactor output without being affected by any one of the K unknown logic values.

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For every combination of K scan chains, K + 1 columns are added to the compactor matrix in one embodiment. Thus, in an example with 100 scan chains, where K = 2, 100 x 99 x 98 divided by 6 (3 x 2 x 1) or almost 160,000 combinations are possible. In an example where K equals 2, K + 1 = 3, so there are almost 480,000 columns that result from taking every combination of scan ins in groups of 3. Thus, for example, every combination of the scan ins may be taken.

This addition of columns results in a matrix with a large number of columns. Each column in the matrix ultimately may correspond to structure in the resulting compactor design in a fashion described hereafter.

In order to create the matrix, a row that corresponds to a chosen scan chain has the values 100… entered into its matrix as new columns. The new columns have the values one then zero, then another zero extending to K + 1 new columns. Thus, in the example where K equals 2, 3 columns are added with values 100 in the first row. The next scan chain in the combination is then assigned the values 010… The row corresponds to the chosen scan chain and the columns correspond to the newly added columns. In an example where K equals 2, the second scan chain in each particular combination is assigned the value 010 in the second row. Then the third scan chain in the combination is chosen and the values 001… are entered into the matrix. Again, the row corresponds to the chosen scan chain and the

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columns correspond to the newly added columns. In a simple example where K equals 2, the numbers 001 are provided as new columns in the third scan chain row of the chosen set of 3. The entries in the remaining rows in the newly added columns may be provided with "don't care" values.

The number of columns can become exceptionally large. However, the number of columns may be reduced using maximum compatibility class problem analysis. This analysis says that any two columns can be merged and represented by a single column if the two columns do not have conflicting 1's and 0's in the same row. Thus, any 1's and 0's that are the same for all the scan lines for a given pair of columns can be reduced and represented by a single column. Don't care values are not material. Thus, a 0 in one column in the same row with a don't care in another column match and a 1 in the same row with a don't care also matches. There is only a conflict if a 1 is matched with a 0 on the same row or a 0 is matched with a 1 on the same row.

One of the merged columns can be eliminated, resulting in a minimum number of columns. It is a necessary and sufficient condition for multiple unknown handling matrixes to match element by element in two columns.

Once the matrix is developed and reduced, all that needs to be done then is to develop the compactor. In each case where a 1 is arranged for a given output in a given

scan in, that scan in is connected through an exclusive OR gate 14 to the indicated output, in one embodiment. Thus, in the case of the matrix shown in Figure 3, because there is a 1 across from scan in 1 and under output 1, an

5   exclusive OR gate connects the scan in 1 to the output 1. Because there is a 1 under output 1 and across from scan in 2, the same exclusive OR gate couples scan in 2 to output 1. This arrangement is repeated to produce the desired number of rows and columns.

10   Referring to Figure 4, in an embodiment implemented in software, initially the maximum number of scan chains that can produce unknown logic values at the same time is set equal to K, as indicated at block 20. The total number of scan chains is set equal to N, as indicated in block 22.

15   Then, based on K, scan chains are added to the compactor matrix, as indicated in block 24. For example, K + 1 columns may be added to the scan chain matrix for each possible combination of K + 1 scan chains. For every combination of K + 1 scan chains, columns may be added to

20   the matrix. Then the number of columns in the matrix may be reduced using maximum compatibility class problem as indicated in block 26.

Thus, the aim is to guarantee the detection of P or fewer errors when K or fewer scan chains produce unknowns.

25   To do so, a reduced matrix is obtained by removing any K rows of the original matrix and columns in which any of

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these K rows have ones. A bit-wise exclusive OR of any P or fewer rows of this matrix must not be all zeros.

In one embodiment, a response compactor may be formed with a plurality of exclusive OR gates arranged to handle any number of scan in errors and unknown logic values. A compactor may handle any number of errors in the same scan cycle. Moreover, in some embodiments, the compactor may have the minimum number of scan outputs. For example, using the maximum compatibility class problem, the number of columns may be reduced to the minimum possible number. This corresponds to having the minimum number of scan outputs.

In some embodiments, the compactor may be coupled to other devices, such as the so-called Intel scan out structure, that may use a shift register. Other devices, including counters, could also be used on the compactor output.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: